

# Reconfigurable and Spectrum Aware Receiver Architecture for Cognitive Radio

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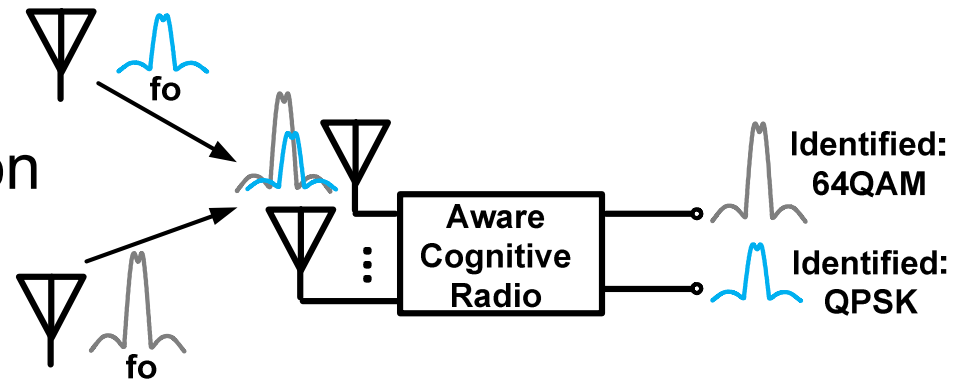
# Outline

- Motivation: Spectrum aware Cognitive Radio
- Overview of system architecture
- Challenges of broadband receivers
- Front-end filtering: N-path filter approach
- Improving the N-path filter
  - T-line N-path filter
  - PN sequence N-path filter
- Conclusions

# Motivation: Spectrum Aware Cognitive Radio

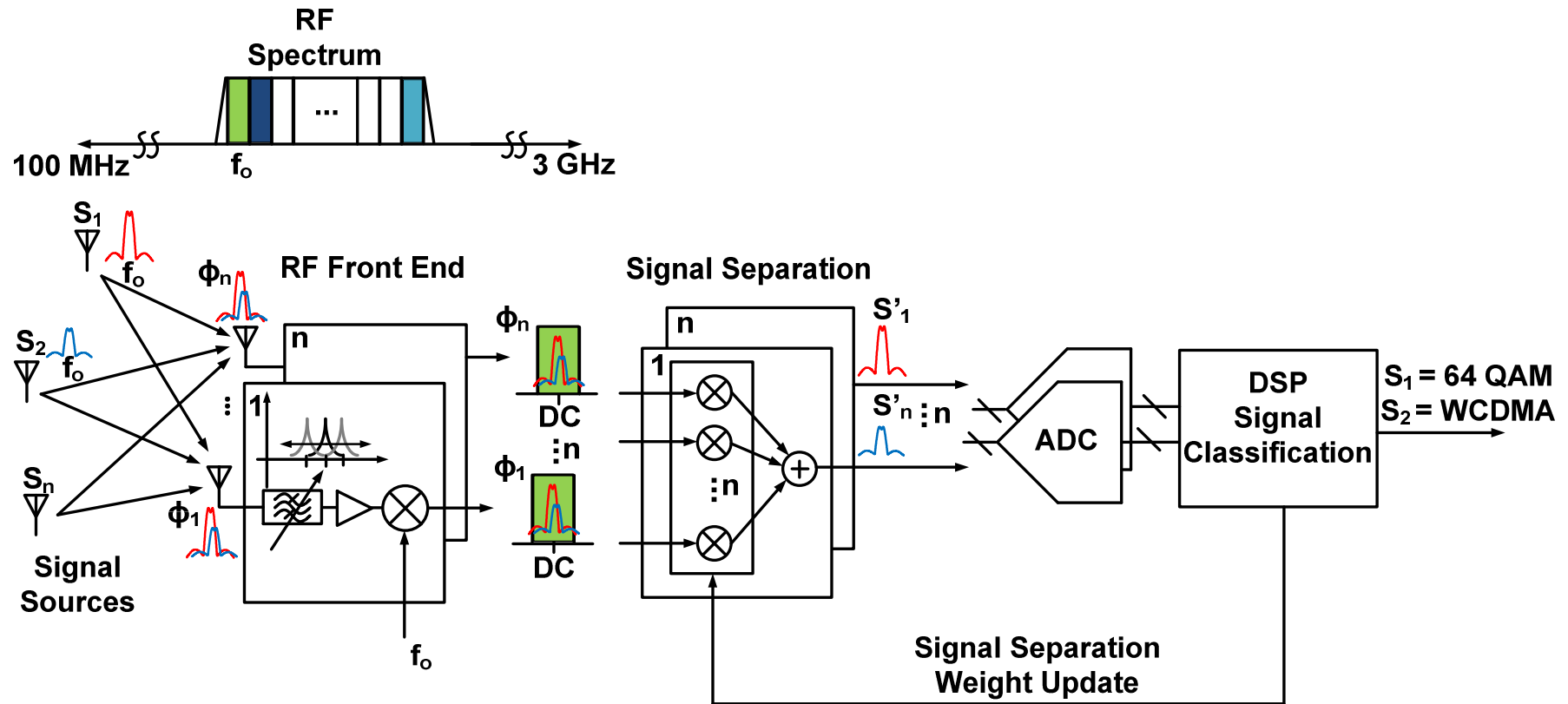
- Application of universal broadband signal classification

- Spectrum aware cognitive radio
- Spectrum surveillance



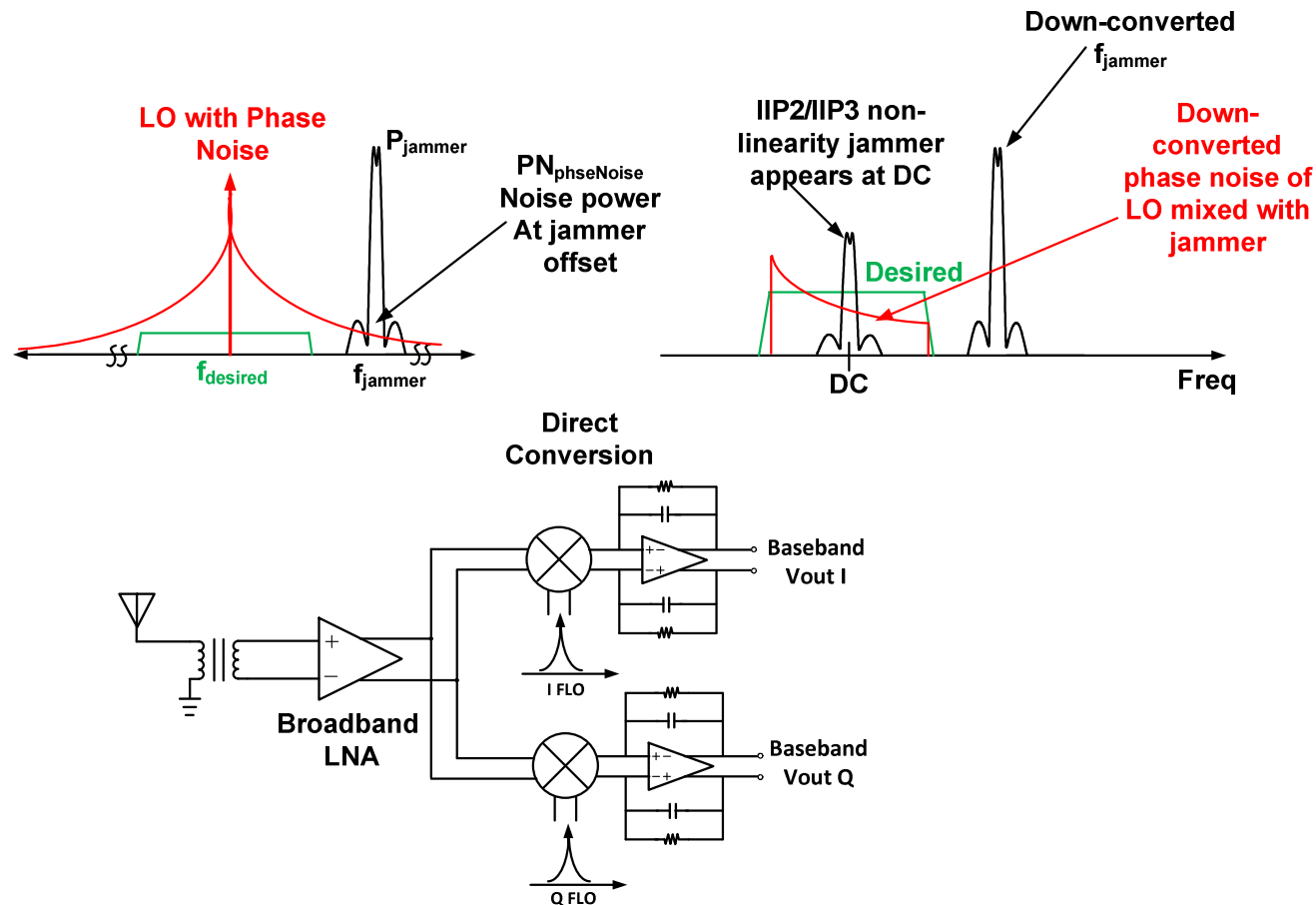
- Requirements of signal classification receiver
  - Robust broadband receiver for multiband coverage
  - Signal separation for classification
  - Wide bandwidth (up to 50 MHz) for multi-standard coverage
  - Low power for mobile applications

# System Architecture of Classification Receiver



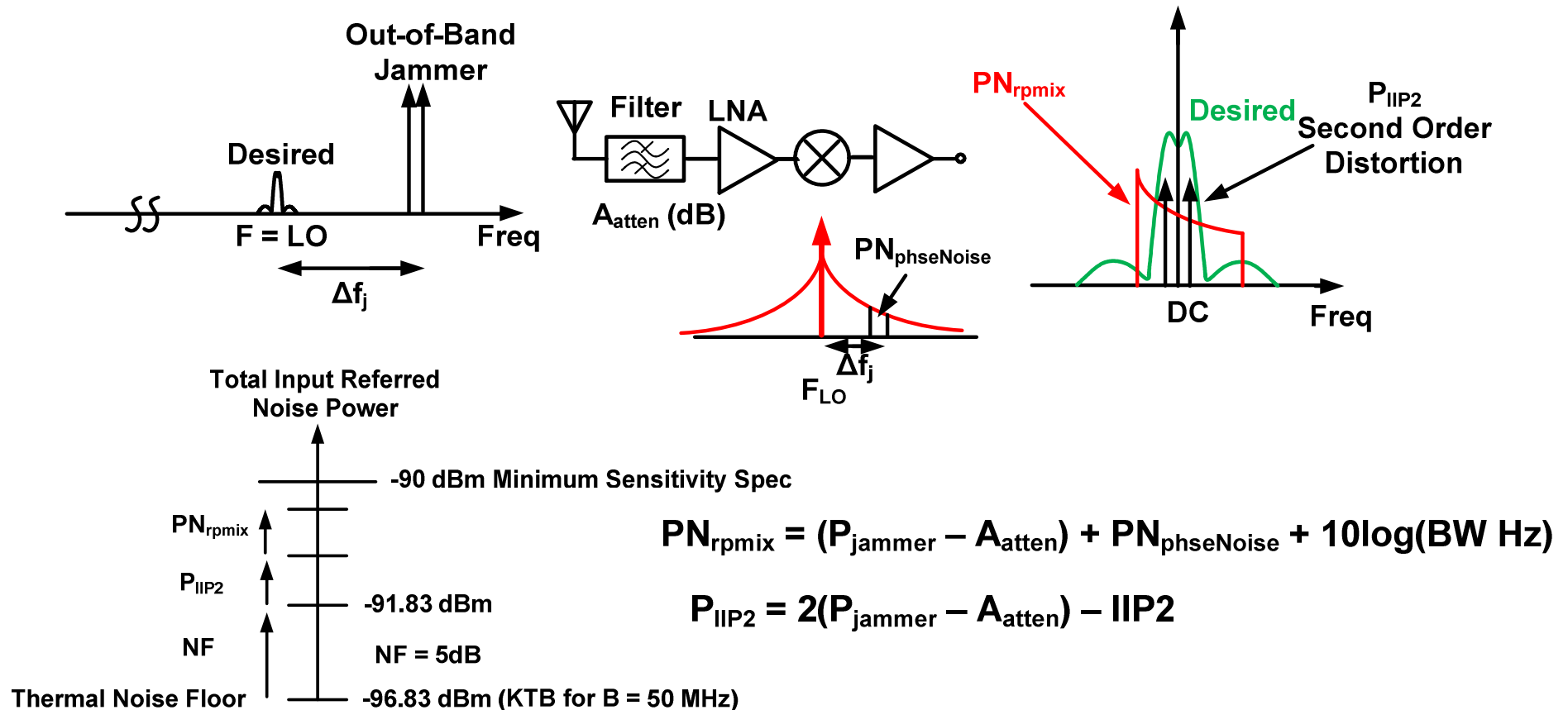
- Multiple Antennas for spatial diversity
- Broadband tunable front-end with reconfigurable filter
- MIMO spectral overlap signal separation
  - Multiplication of received matrix with learned weights that approximates inverse of the transmission channel
- ADC and DSP feedback learning

# Broadband Receiver with Jammer Challenge



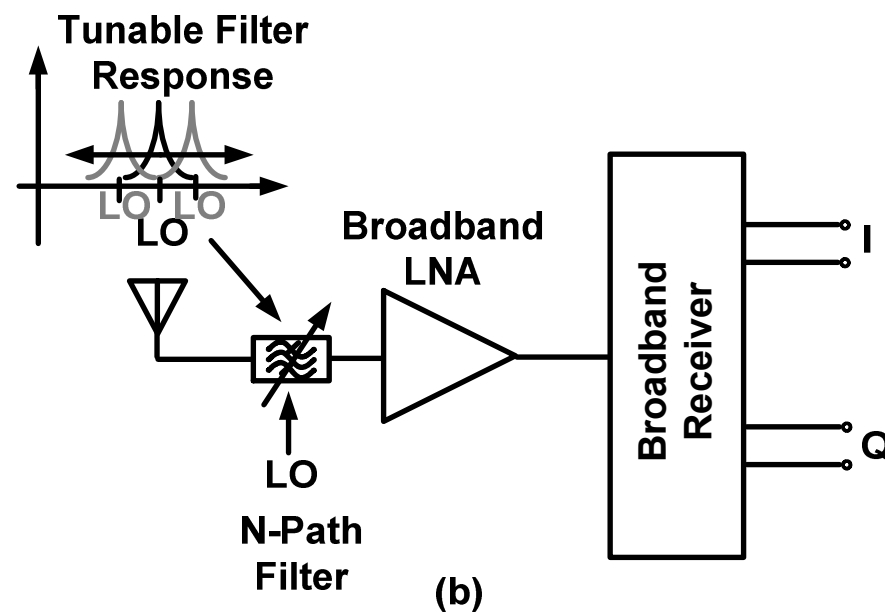
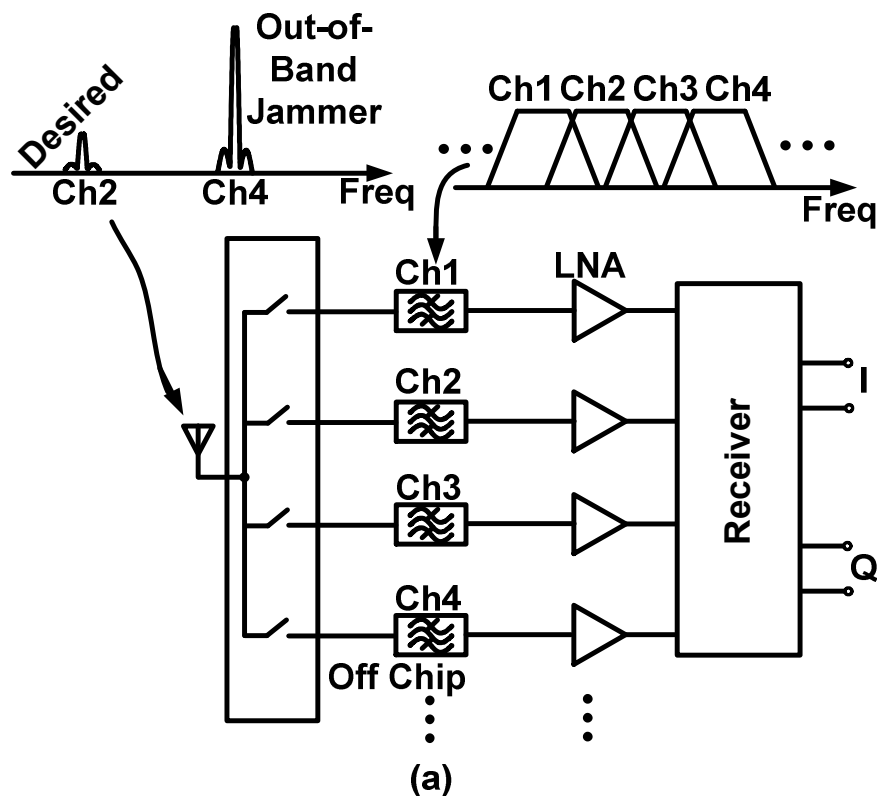
- Jammer coupled with receiver non-idealities (LO phase noise, finite linearity IIP2 and IIP3) raises noise floor.
- A highly tunable frequency band selective filter for out-of-band jammer rejection is desirable.

# Direct Conversion Receiver Filter System Level Calculation



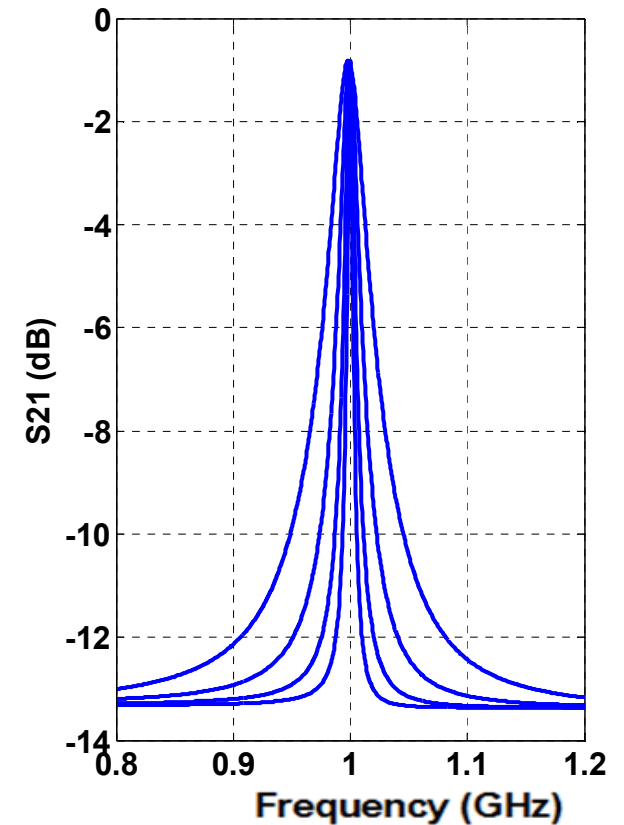
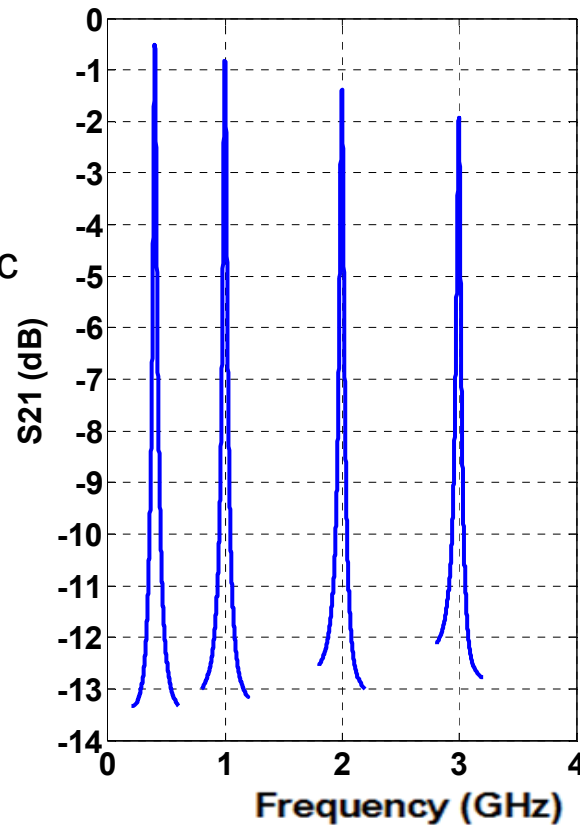
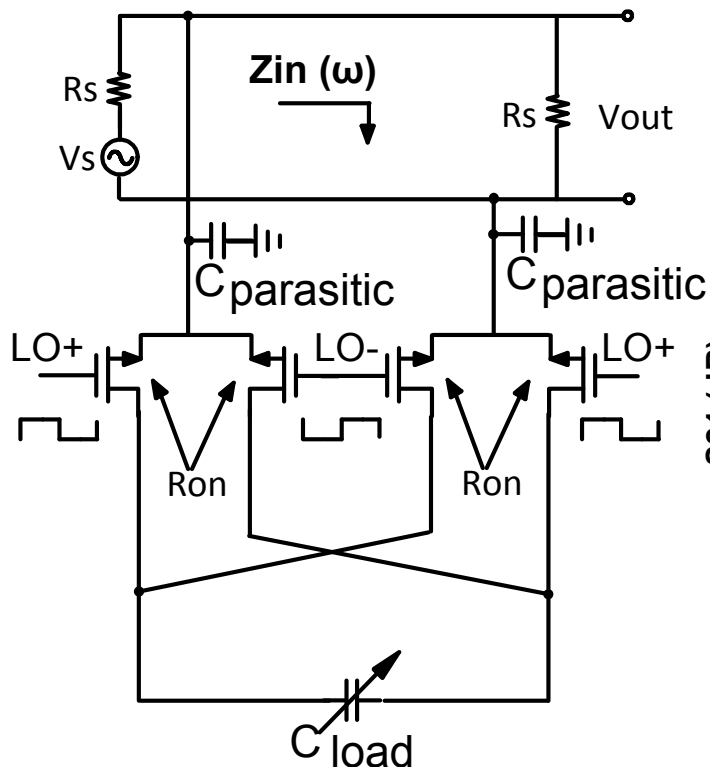
- With  $P_{jammer} = +0 \text{ dBm}$ ,  $NF = 5 \text{ dB}$ ,  $IIP2 = +50 \text{ dBm}$ , oscillator phase noise of  $-162 \text{ dBc/Hz}$  at jammer offset, and Filtering of  $30 \text{ dB}$  gives the sensitivity as:  $-91.75 \text{ dBm}$ .
- Need approximately  $A_{atten} = 30 \text{ dB}$  of filtering for  $0 \text{ dBm}$  jammer.

# Broadband Tunable Receiver with N-path Filter Approach



- (a) Multiple off-chip SAW filter approach
- (b) Tunable fully integrated filter approach [1]

# N-path Filter



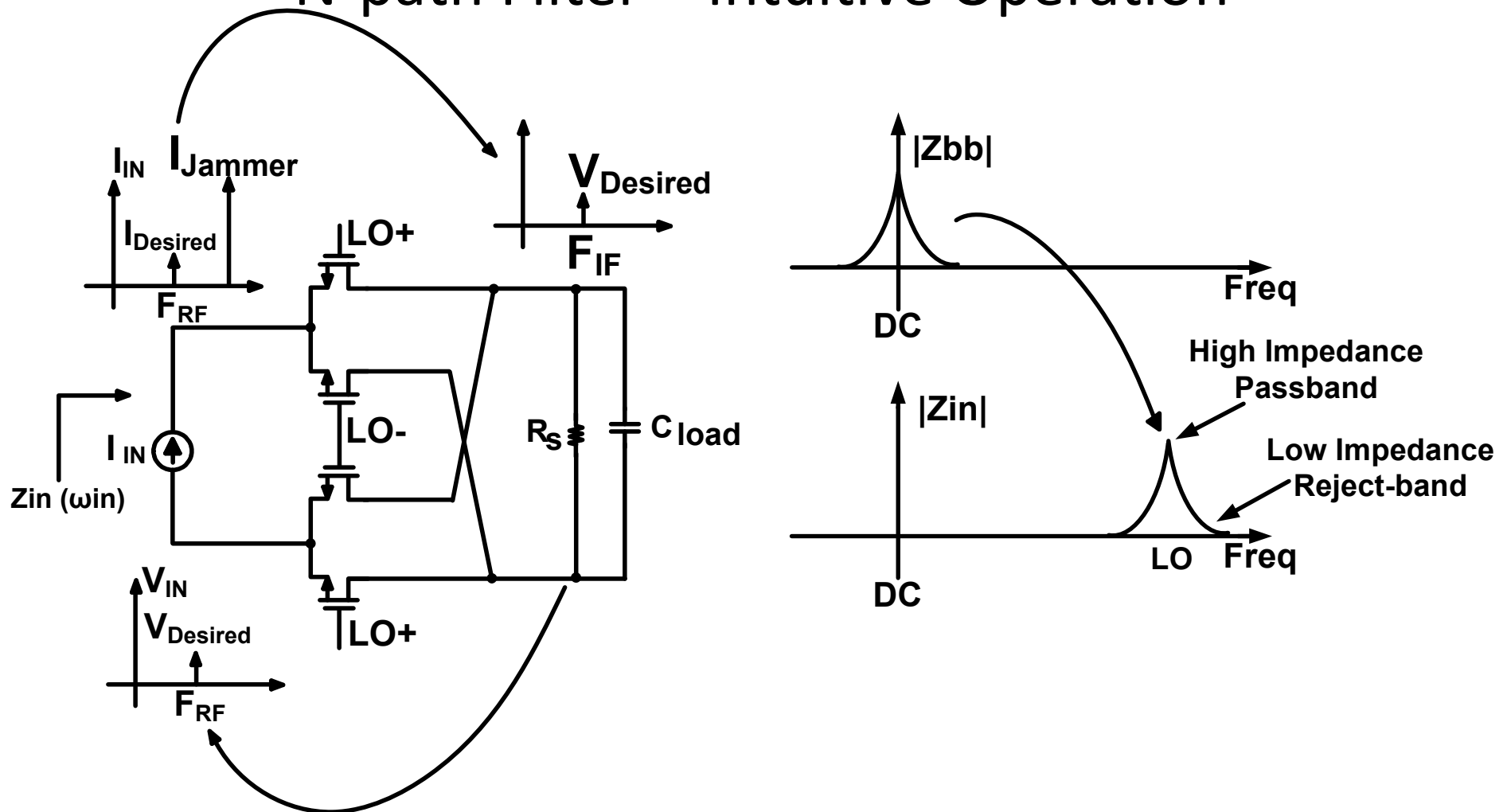
$$Z_{in}(\omega) \approx Z_{C_{parasitic}}(\omega) \parallel (Z_{Load}(\omega_{LO} - \omega) + 2R_{on})$$

65 nm RFCMOS / 50 ohm system

- Baseband capacitive impedance translated to  $\omega_{LO}$
- Out-of-band rejection limited by the resistance and parasitic capacitance of the CMOS switch

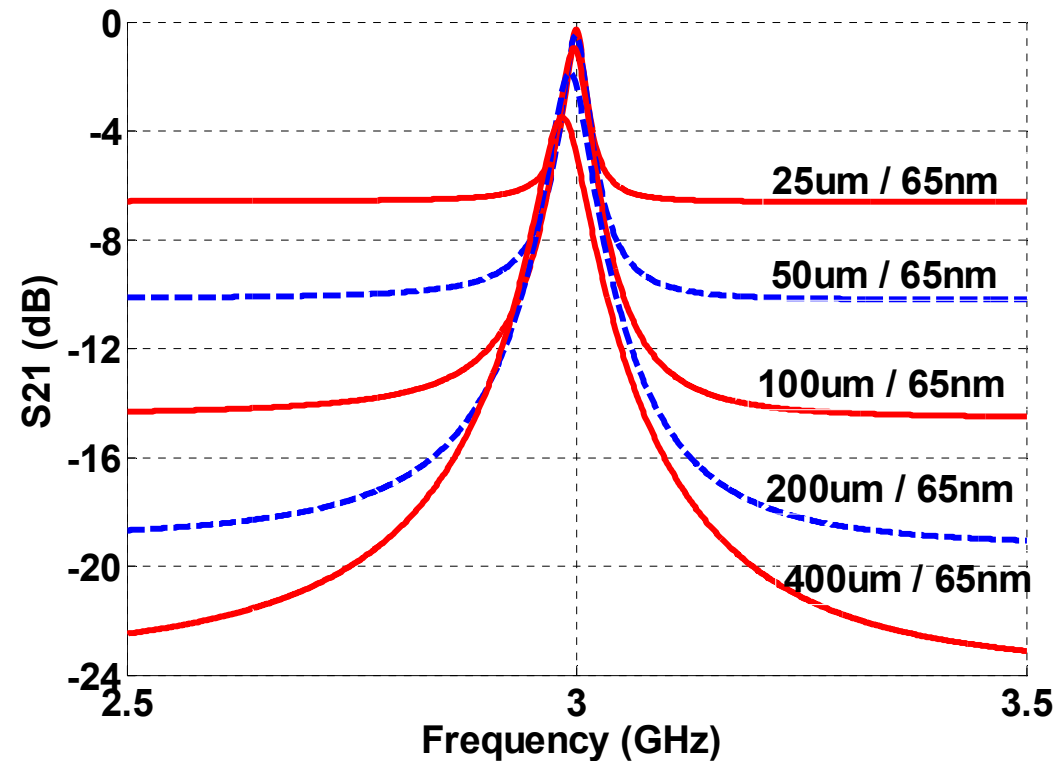
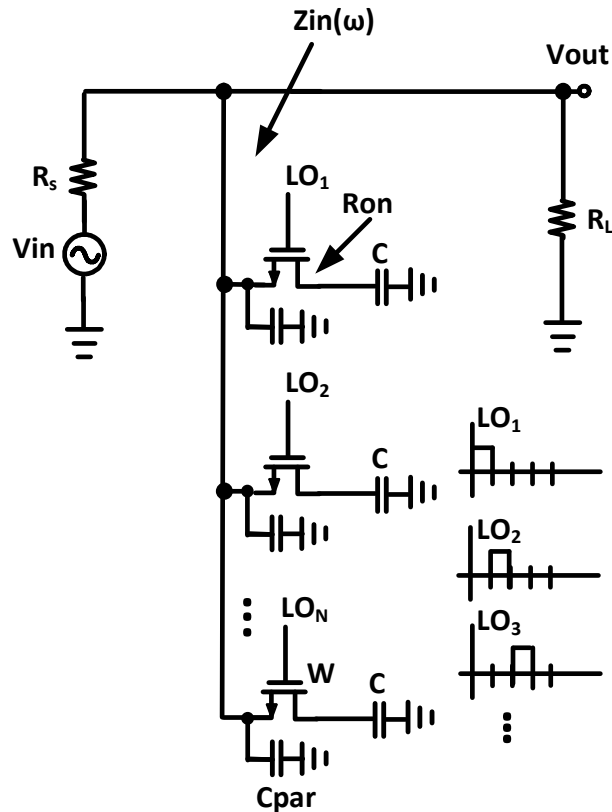


# N-path Filter – Intuitive Operation



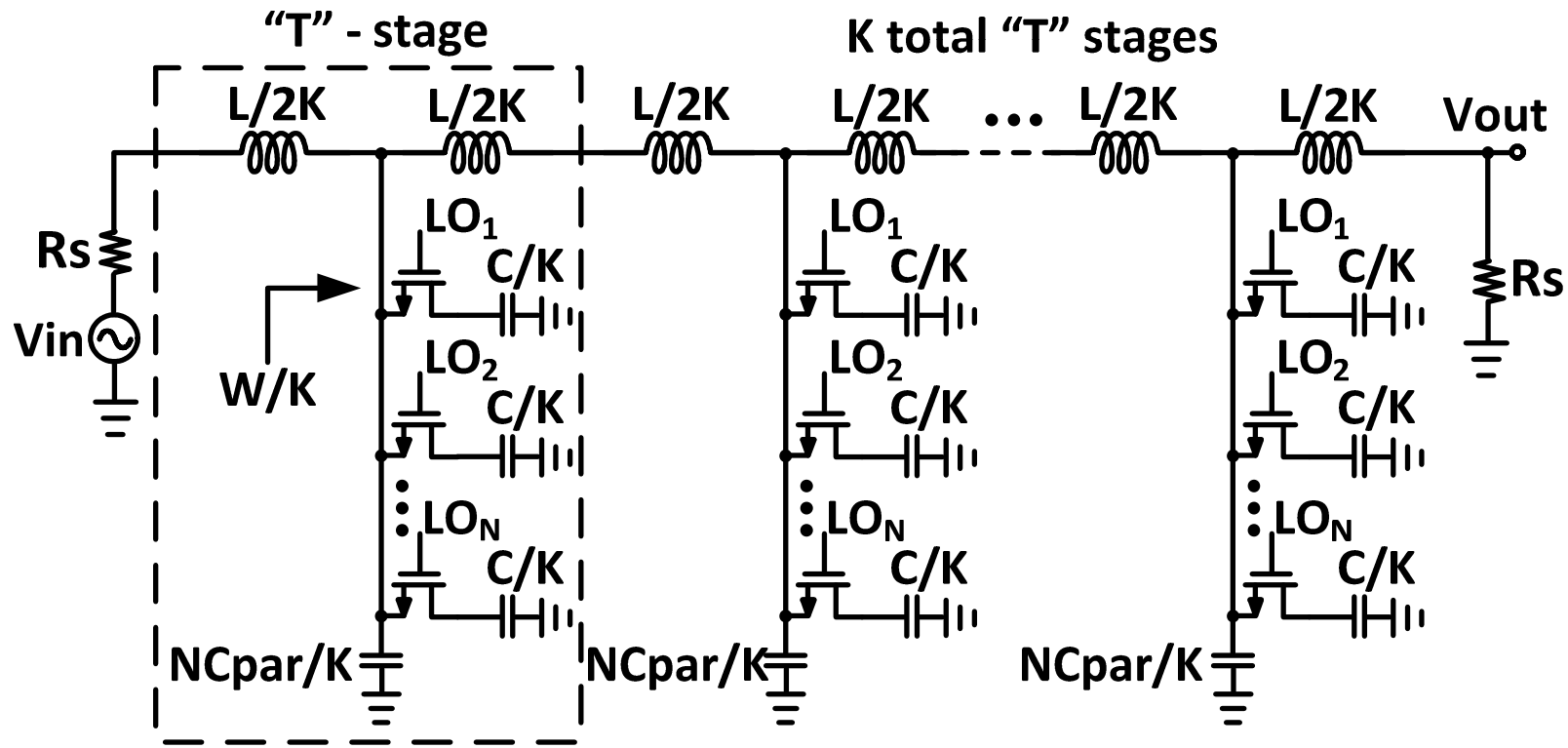
- Passive mixer translates baseband impedance to switching frequency [2].

# N-Path Filter Fundamental Limitation



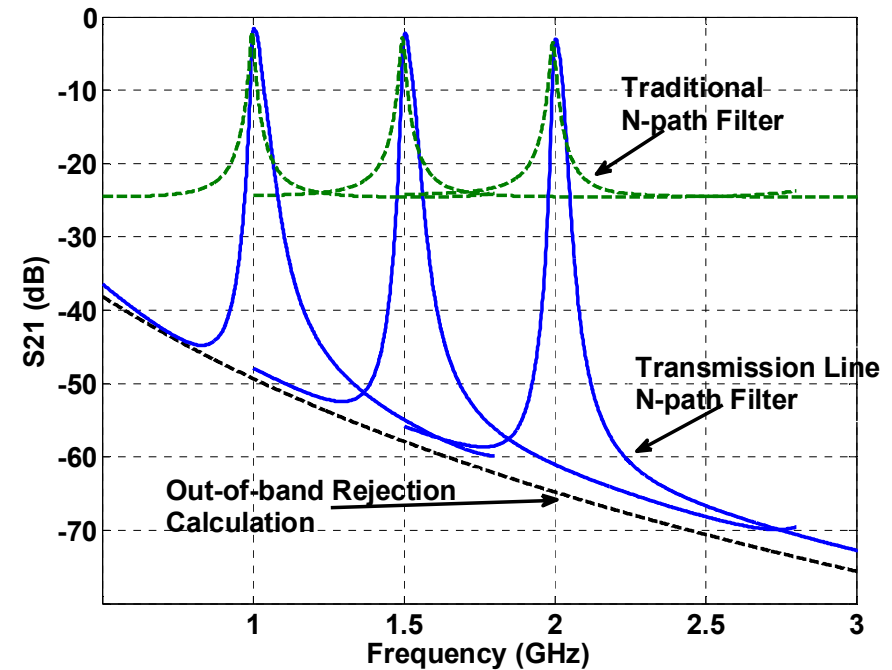
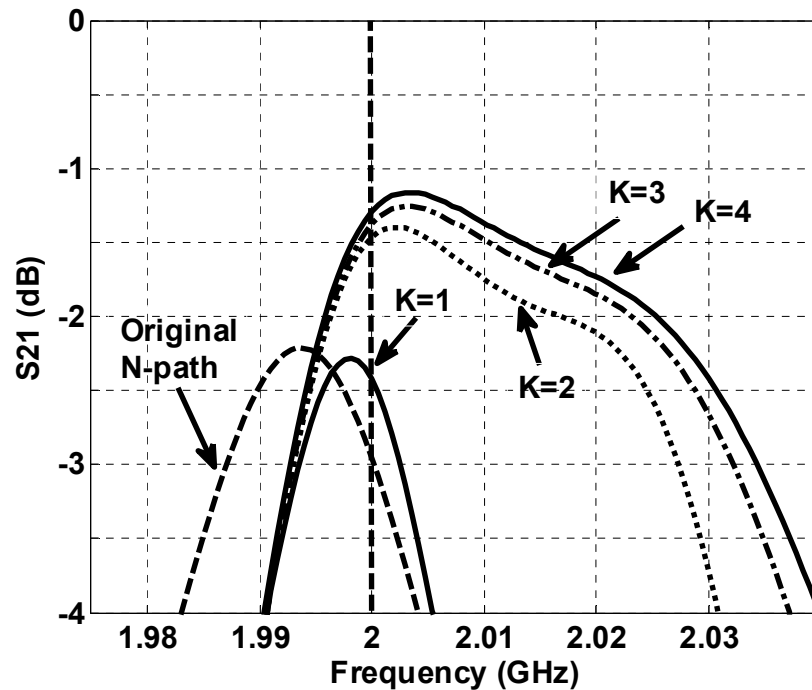
- Pass-band loss is approximately  $S_{21} \approx 1 / (1 + sR_sNC_{par})$
- Out-of-band rejection is limited by switch  $R_{on}$ .
- Parasitic capacitance shifts peak  $S_{21}$  to lower frequency.

# Proposed Transmission Line N-path Filter



- Parasitic capacitance absorbed into transmission line.
- Out-of-band rejection improved by further low-pass filter created by  $L$  and  $R_{on}$ .
- Improves tradeoff between pass-band loss and out-of-band rejection.

# T-Line N-path Filter Simulation Results

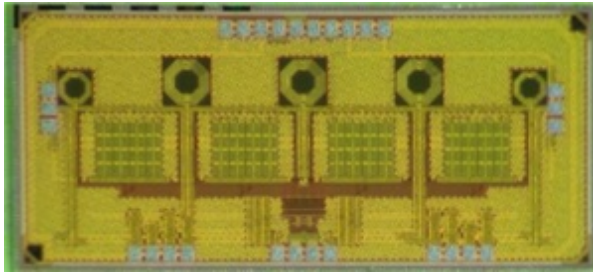


$$S_{21}(S) \approx 8R_s R_{on}^K / (S^{K+1} L^{K+1})$$

Out-of-band rejection approximation with T-line

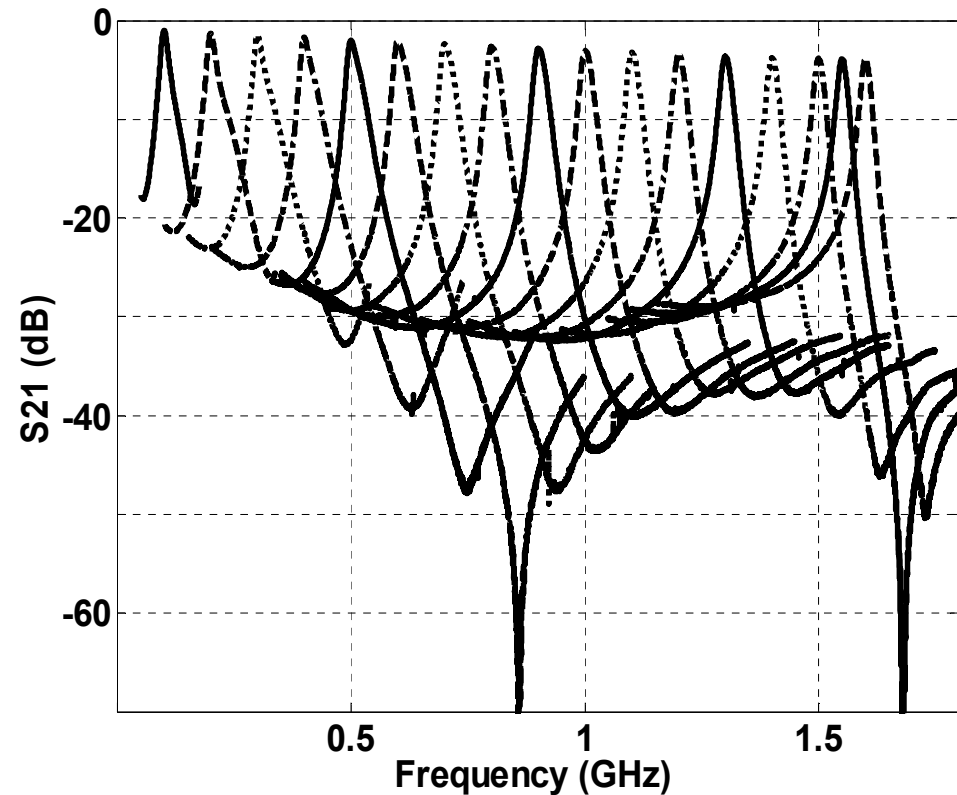
- Parasitic capacitance absorbed into transmission line improving in-band insertion loss.
- Out-of-band rejection improved by further low-pass filter created by L and  $R_{on}$ .

# T-Line N-path Filter Measurement Results



Chip micrograph (3mm x 1.4mm).

$K = 4$ ,  $L/K = 3.8 \text{ nH}$ ,  $Q_{\text{ind}} = 16$  at 2 GHz, Selfres = 7.5 GHz



- Parasitic capacitance absorbed into transmission line improving in-band insertion loss.
- Out-of-band rejection improved by further low-pass filter created by  $L$  and  $R_{\text{on}}$ .

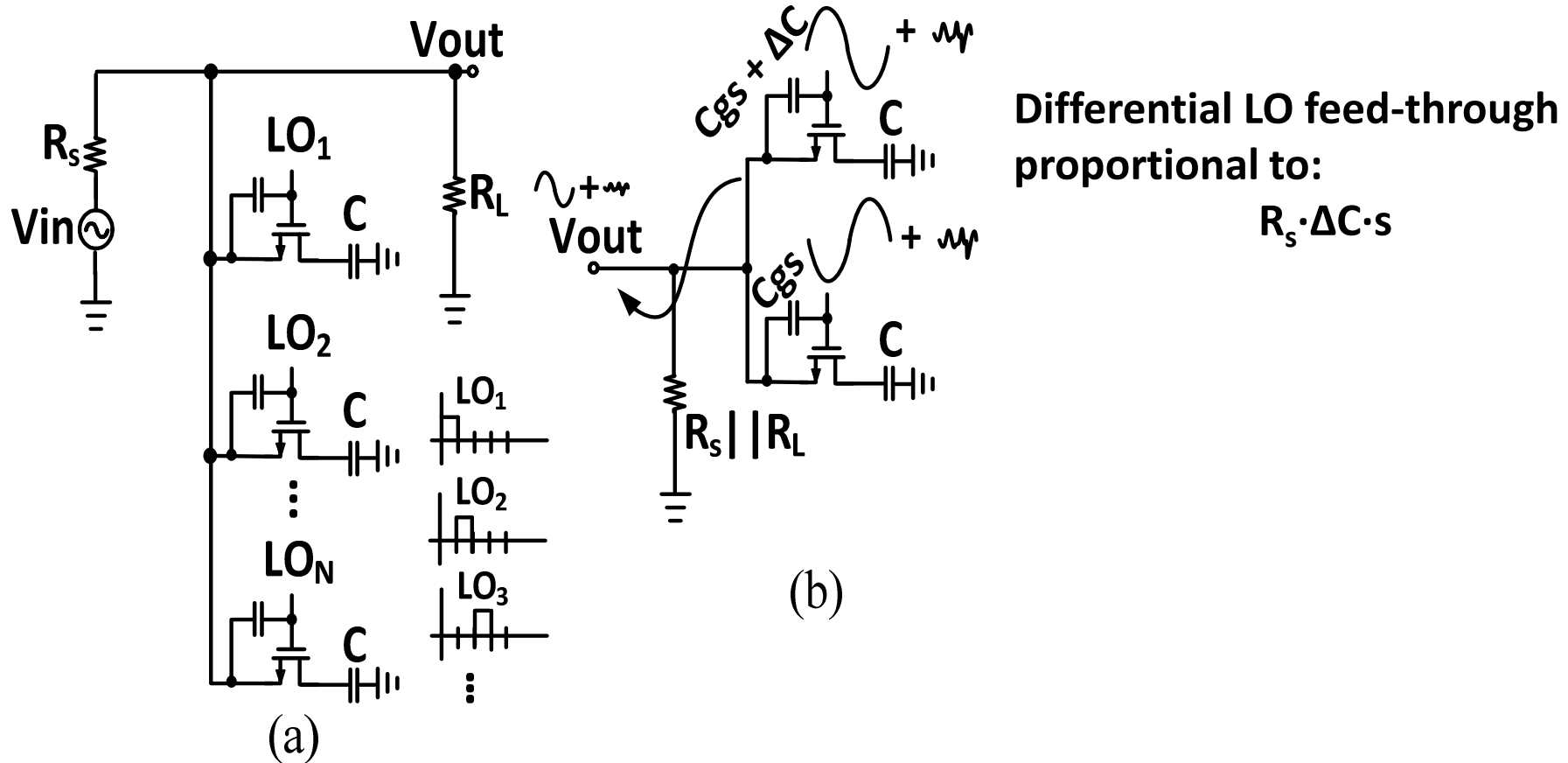
# T-Line N-path Filter Measurement Summary

	<b>This Work</b>	<b>Ghaffari Nauta 2011</b>	<b>Darvishi Nauta 2013</b>	<b>Darvishi Nauta 2013</b>	<b>Thomas Larson 2014</b>
<b>Technology</b>	<b>65 nm</b>	<b>65 nm</b>	<b>65 nm</b>	<b>65 nm</b>	<b>65 nm</b>
<b>Frequency Range</b>	<b>0.1–1.6 GHz</b>	<b>0.1–1 GHz</b>	<b>0.4–1.2 GHz</b>	<b>0.1–1.2 GHz</b>	<b>0.5-1.5 GHz</b>
<b>Out-of-band Rejection</b>	<b>30-50 dB</b>	<b>15 dB</b>	<b>55 dB</b>	<b>59 dB</b>	<b>31-53 dB</b>
<b>In-band IIP3</b>	<b>+29 dBm</b>	<b>+14 dBm</b>	<b>+9 dBm</b>	<b>-12 dBm</b>	<b>+4.9 dBm</b>
<b>Jammer P1dB Compression</b>	<b>+ 11 dBm</b>	<b>&gt; +2 dBm</b>	<b>&lt; +2 dBm</b>	<b>+ 7 dBm</b>	<b>+7 dBm</b>
<b>NF</b>	<b>1.5–5.4 dB</b>	<b>3–5 dB</b>	<b>9.7-10.5 dB</b>	<b>2.8 dB</b>	<b>5-10 dB</b>
<b>Power</b>	<b>30-200 mW</b>	<b>2–16 mW</b>	<b>21.4 mW</b>	<b>15-48 mA</b>	<b>50-200 mW</b>

The diagram illustrates a receiver architecture with a tunable filter response. At the top, a graph shows the **Tunable Filter Response** with  $|Z_{in}|$  on the vertical axis and frequency on the horizontal axis. It features two overlapping resonance curves centered at  $L_0$  and  $LO$ , with a horizontal double-headed arrow indicating the tuning range. The main circuit includes an antenna connected to a node that branches into a **Leakage** path (indicated by a curved arrow) and the input of an **N-Path Filter**. The **N-Path Filter** is represented by a circle with an 'X' and is loaded with  $xM$  parallel branches, each containing a capacitor  $C_{Load}$ . The output of the filter is connected to a **Broadband LNA** (Low Noise Amplifier), which also has a **Leakage** path (indicated by a curved arrow). The LNA output is connected to a **Broadband Receiver**, which provides **I** and **Q** outputs. Two  **$N$  Phase LO** (Local Oscillator) signals are shown as frequency spectra with components at  $LO$ ,  $2LO$ , and  $3LO$ . One  **$N$  Phase LO** signal is connected to the **N-Path Filter**, and the other is connected to the antenna via a leakage path.

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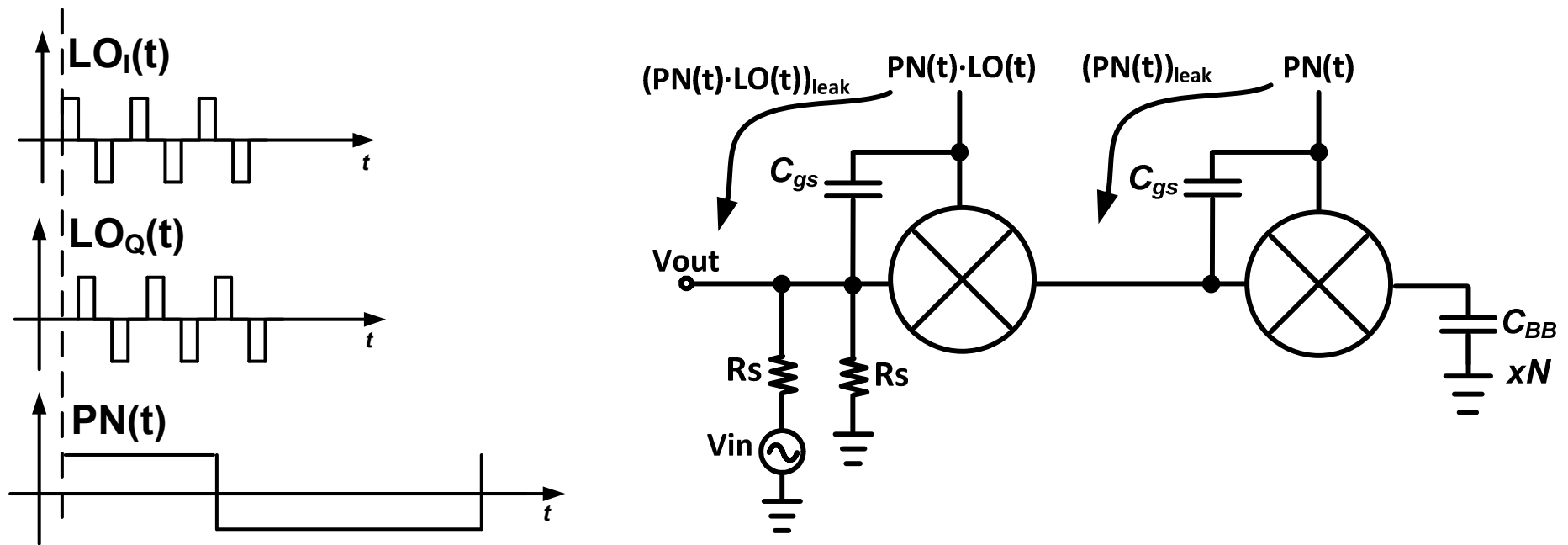
# Mechanism of LO Leakage Radiation



- **Any** asymmetry leads to LO leakage.
- Differential LO feed-through directly proportional to parasitic capacitance mismatch and frequency.



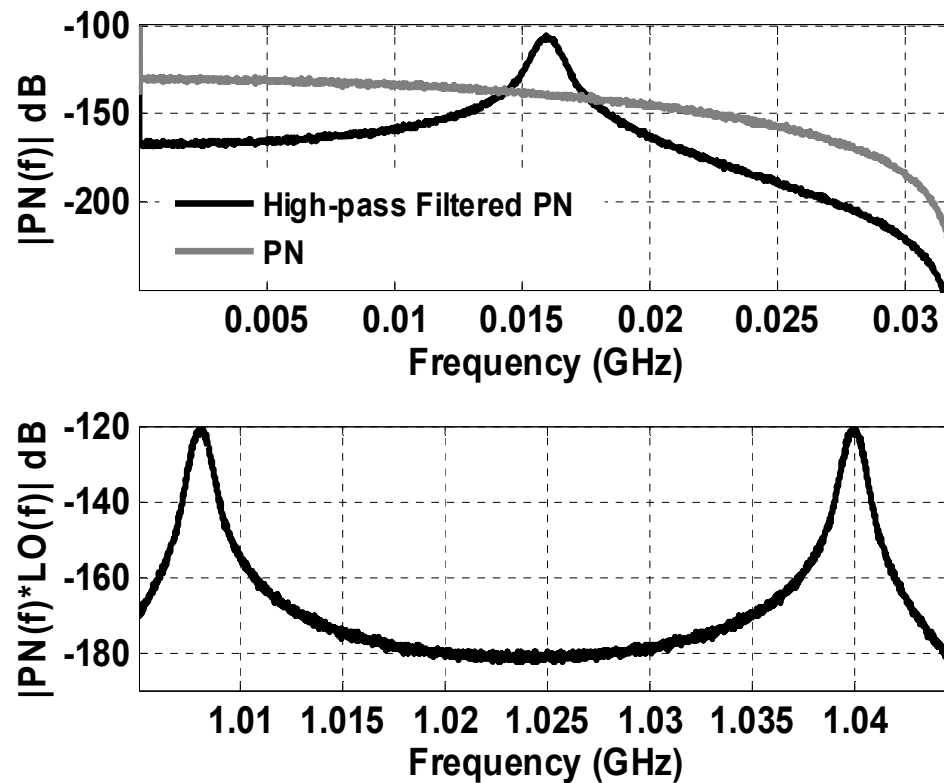
# Proposed N-path Filter with Pseudorandom Clocking



$$\text{Leakage}_{\text{total}} \approx \underbrace{(\text{PN}(t) \cdot \text{LO}(t))_{\text{leak}}}_{\text{Broadband Leakage}} + \underbrace{\{\text{PN}(t) \cdot \text{LO}(t)\} \cdot (\text{PN}(t))_{\text{leak}}}_{\text{Tonal Leakage}}$$

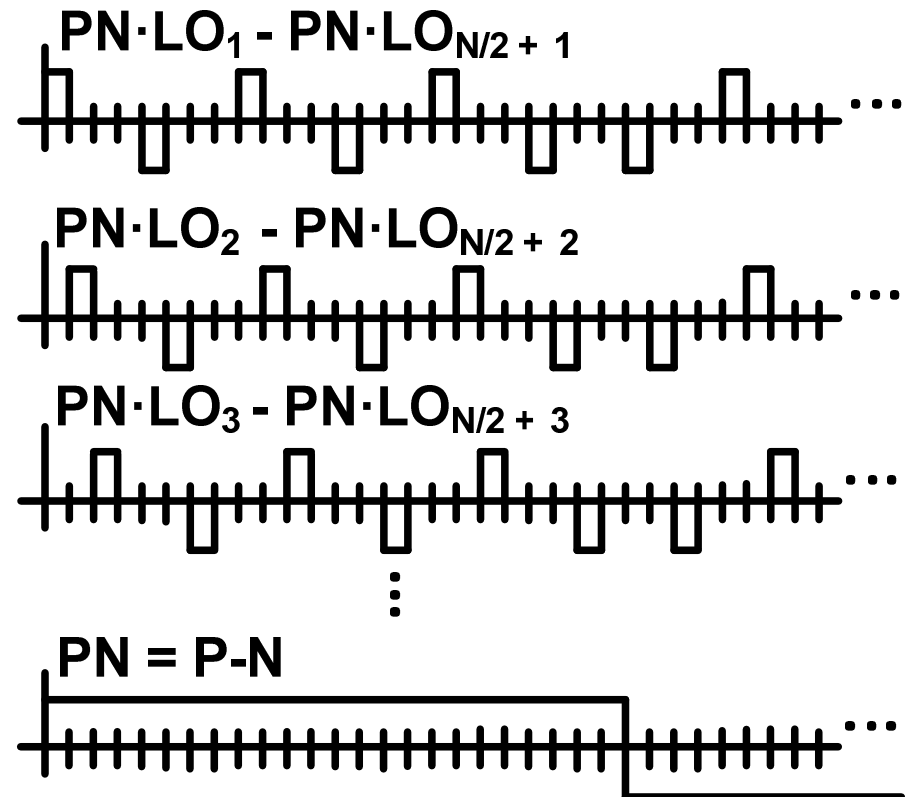
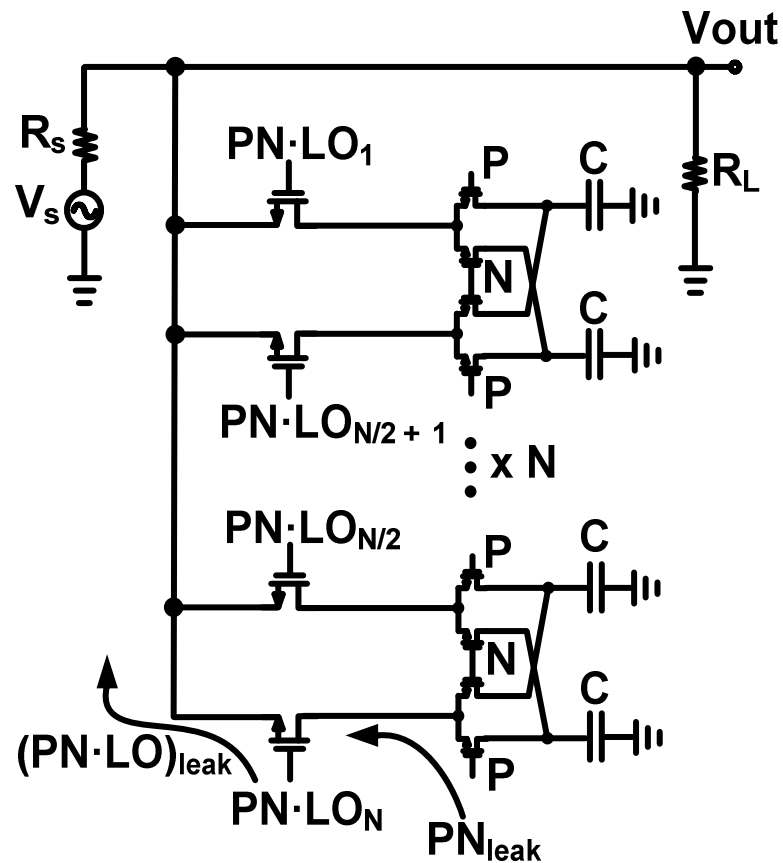
- Same transfer function utilizing:  $\text{LO}(t) \cdot \text{PN}(t) \cdot \text{PN}(t) = \text{LO}(t)$ .
- $\text{PN}(t)$  is a low frequency, broad-spectrum PN sequence.

# Simulated PN Sequence Spectrum Shaping



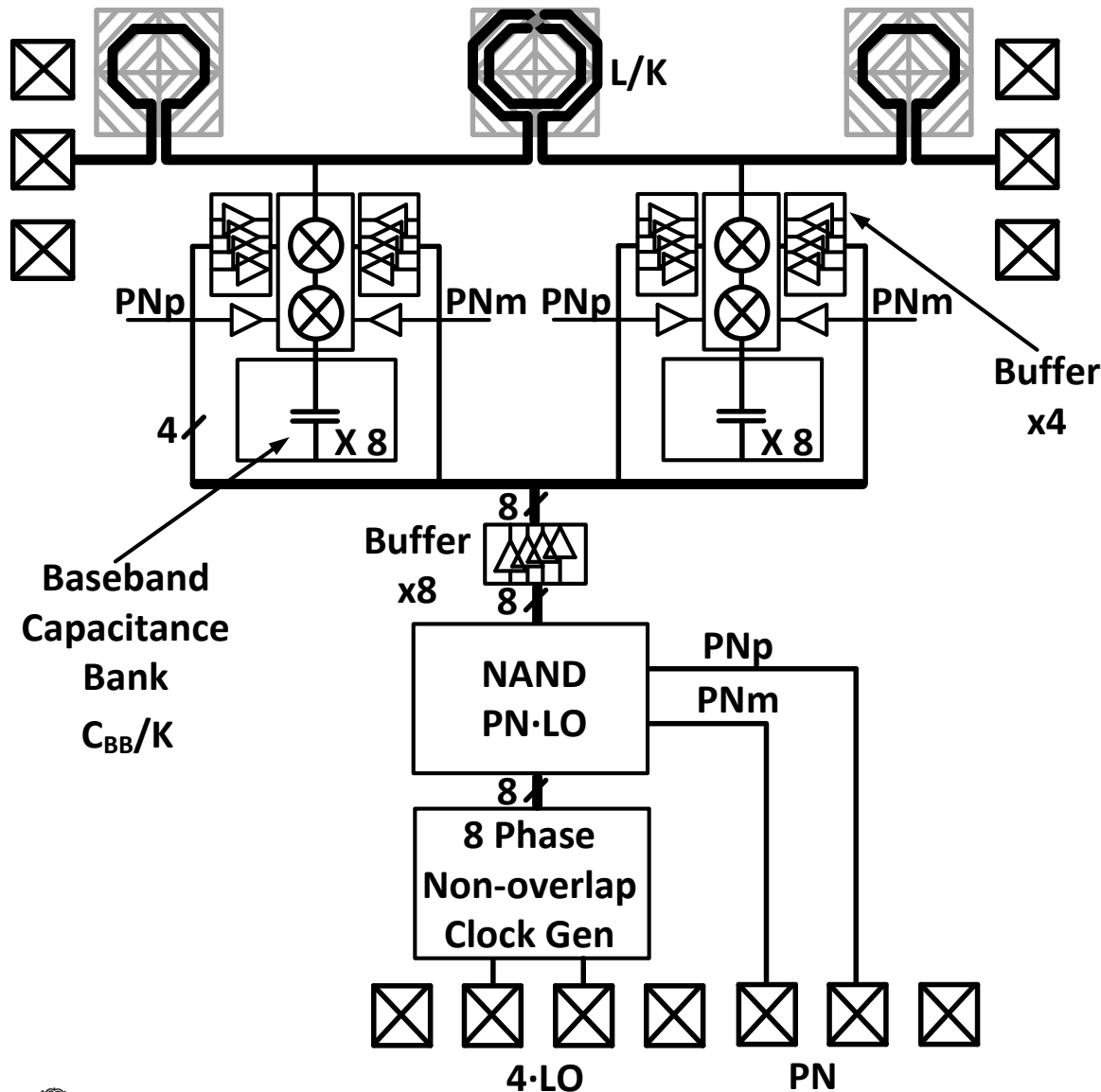
- Simulation of high-pass filtered PN (using iterative digital high pass:  $1 - Z^{-1}$ ).
- Simulation of filtered  $PN(t) \cdot LO(t)$  giving in-band null.

# PN N-path Bandpass Implementation



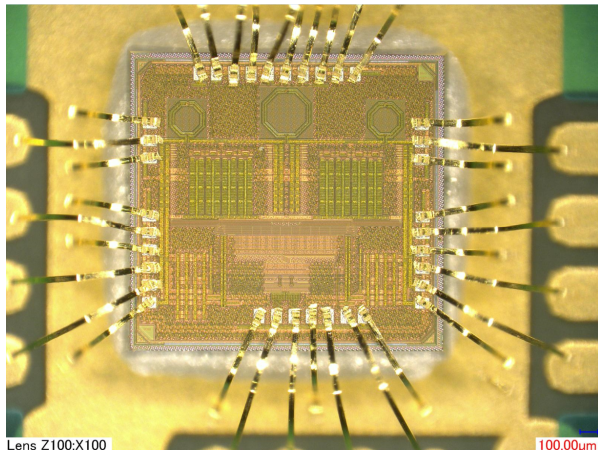
- Differential PN mixer to single-ended interface.

# Two Stage T-Line N-Path Filter

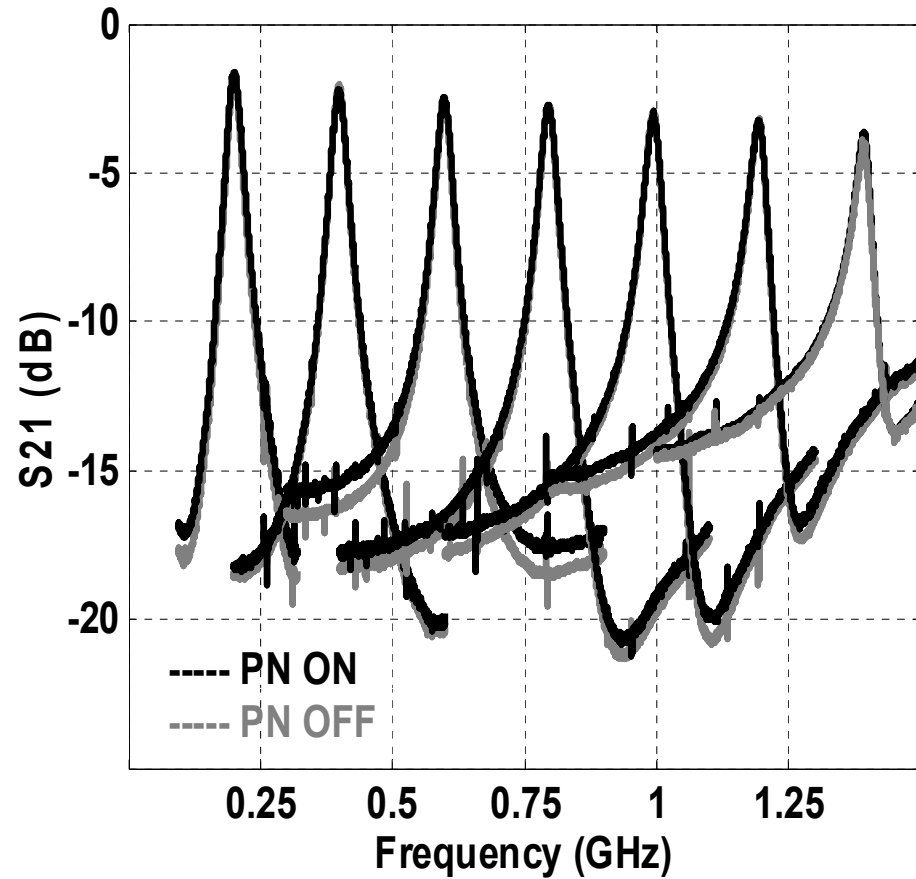
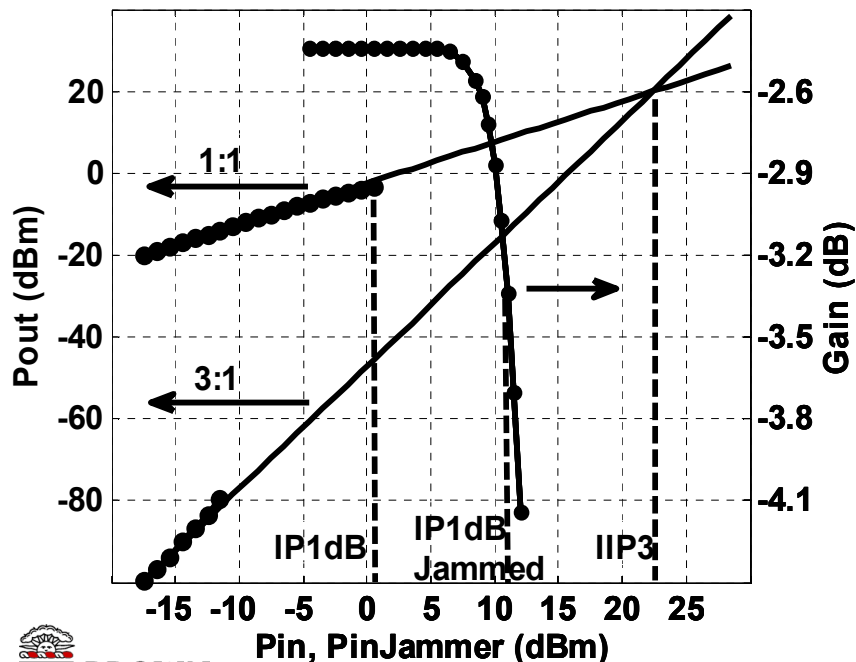


- T-Line N-path Filter Technique [5].
  - Ideally improve insertion loss
  - Ideally improve rejection
- Two Stage Design.

# PN N-path Filter Measured Results

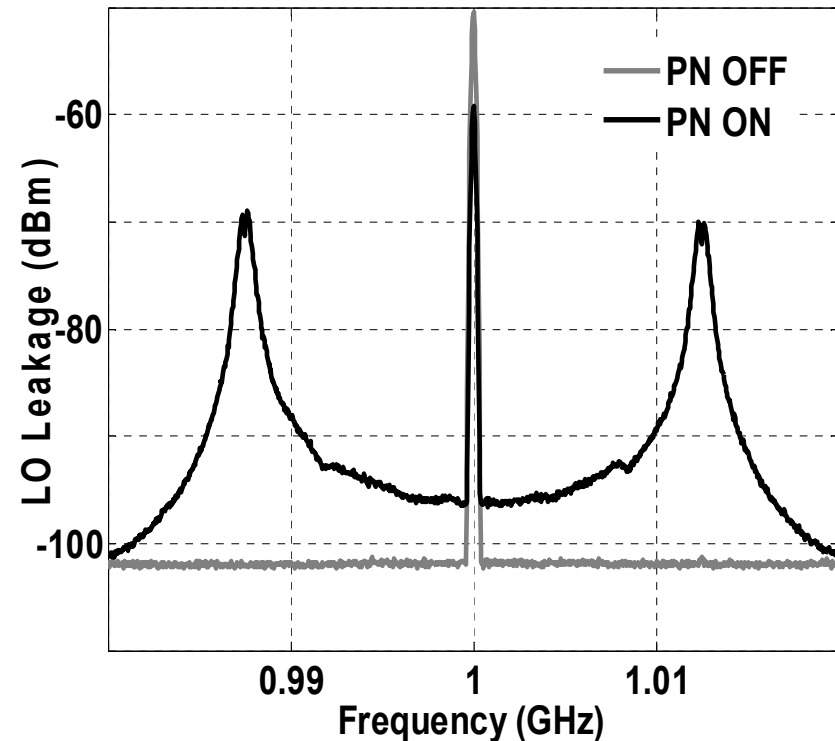
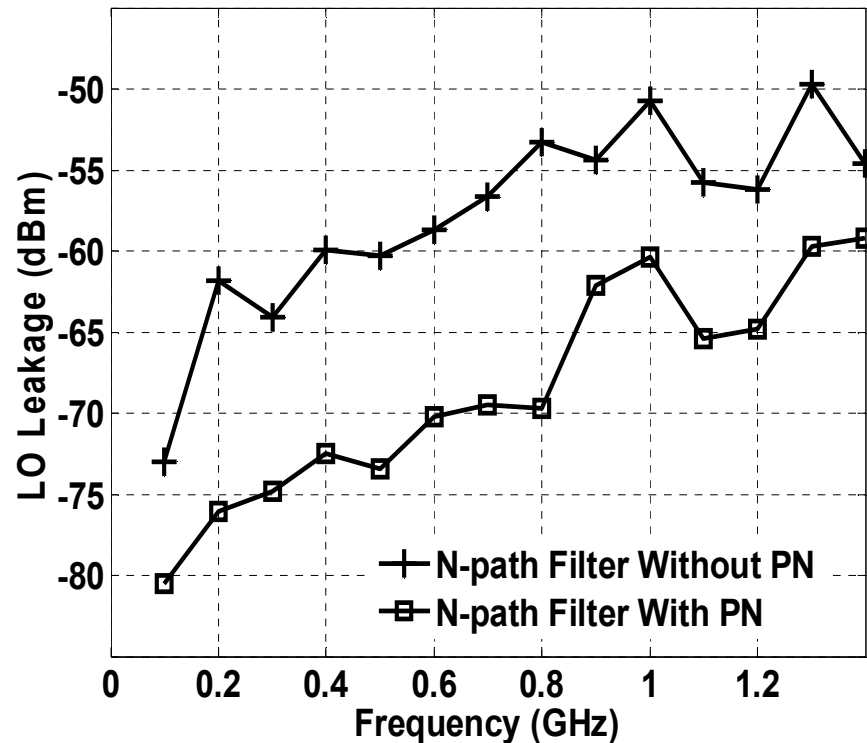


Chip micrograph (1.1mm x 1mm) in 65nm CMOS ribbon bonded to PCB.



- Minimal degradation with PN ON and OFF.
- Jammer IP1dB compression +11 dBm (600 MHz offset), In-band IIP3 +22 dBm.

# Measured LO Leakage Improvement



Measured in-band LO leakage at 1 GHz  
(RBW = 200 KHz, span = 40 MHz).

- LO Leakage improvement: 10 to 15 dB.
- High-pass filtered PN sequence spreads LO leakage replicating expected spreading shape.

# PN N-path Filter Measurement Summary

	<b>This Work</b>	<b>Darvishi Nauta 2013</b>	<b>Darvishi Nauta 2013</b>	<b>Thomas Larson 2014</b>
<b>Technology</b>	<b>CMOS 65 nm</b>	<b>CMOS 65 nm</b>	<b>CMOS 65 nm</b>	<b>CMOS 65 nm</b>
<b>Frequency Range</b>	<b>0.1–1.4 GHz</b>	<b>0.4–1.2 GHz</b>	<b>0.1–1.2 GHz</b>	<b>0.1-1.6 GHz</b>
<b>Out-of-band Rejection</b>	<b>15 dB</b>	<b>55 dB</b>	<b>59 dB</b>	<b>30-50 dB</b>
<b>In-band IIP3</b>	<b>+22 dBm</b>	<b>+9 dBm</b>	<b>-12 dBm</b>	<b>+23 dBm</b>
<b>Jammer IP1dB Compression</b>	<b>+11 dBm</b>	<b>&lt; +2 dBm</b>	<b>+ 7 dBm</b>	<b>+10.1 dBm</b>
<b>LO Leakage</b>	<b>-60 to -80 dBm</b>	<b>&lt; -60 dBm</b>	<b>-</b>	<b>-60 dBm</b>
<b>NF</b>	<b>2-5 dB</b>	<b>9.7-10.5 dB</b>	<b>2.8 dB</b>	<b>2.2-5.4 dB</b>

# Conclusions

- A broadband signal classification receiver faces many challenges, namely: front-end filtering
- Presented a broadband tunable T-line N-path filter that improves in-band insertion loss and out-of-band rejection of the traditional N-path filter
- Presented a PN sequence N-path filter that improves spurious leakage of the traditional N-path filter



# References/Questions?/Thank You!

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2. A. Mirzaei; H. Darabi; D. Murphy, "Architectural evolution of integrated M-phase high-Q bandpass filters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol.59, no.1, pp.52-65, Jan. 2012.
3. S. Jayasuriya; Dong Yang; A. Molnar, "A baseband technique for automated LO leakage suppression achieving  $< -80\text{dBm}$  in wideband passive mixer-first receivers," *IEEE Proceedings of the Custom Integrated Circuits Conference (CICC)*, vol., no., pp.1,4, 15-17 Sept. 2014.
4. Andrews, C.; Molnar, A.C., "A Passive Mixer-First Receiver With Digitally Controlled and Widely Tunable RF Interface," *IEEE Journal of Solid-State Circuits*, vol.45, no.12, pp.2696,2708, Dec. 2010.
5. Thomas, C.M.; Larson, L.E., "A 65 nm CMOS tunable 0.1-to-1.6 GHz distributed transmission line N-path filter with +10 dBm blocker tolerance," *IEEE Proceedings of the Custom Integrated Circuits Conference (CICC)*, vol., no., pp.1,4, 15-17 Sept. 2014.
6. Thomas, C.M.; Larson, L.E., "A pseudorandom clocking scheme for a CMOS N-path bandpass filter with 10-to-15 dB spurious leakage improvement," *IEEE Proceedings of the Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, 2015.